REMARKS

Claims 1-14 are pending in the application. Claims 6-9 are objected to and are indicated as containing allowable subject matter by the Examiner. Claims 1-5 and 10 are rejected. New claims 11-14 have been added. Reconsideration of claims 1-14 is respectfully requested.

Claim Rejections – 35 USC § 102

Claims 1-5, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Parker (U.S. Patent No. 6,307,783). The applicants disagree.

Parker does not teach each and every element of claim 1. Claim 1 recites the element of *a voltage level detector* configured to generate a power-up signal (emphasis added). Parker does not teach this element.

The Examiner has taken the position that the high voltage circuit (120) of Parker discloses the voltage level detector element. However, the high voltage circuit (120) "generates the voltages necessary for proper reading, programming an erasure of the memory device (100)" see Parker col. 3, lines 33-39. The high voltage circuit (120) is not a voltage level detector because it does not detect a voltage level. In fact, according to Figure 1 of Parker, the only inputs to the high voltage circuit (120) are the ALE (address latch enable), CLE (command latch enable), SE#, and WP# (write protect pin) signals, none of which provide a voltage to be detected by the high voltage circuit (120).

Furthermore, Parker relates generally to improvements in detecting data stored in multi-level NAND memory cells; see Parker col.1, lines 40-45. Detecting data stored in cells of both multi-level NAND memory cells and conventional NAND memory cells is accomplished by applying a voltage and detecting whether *current* flows (also specifically see col. 4 lines 15-27 of Parker). Therefore any detector in Parker is *a current detector*. In contrast, the present invention requires a voltage level detector, for one example see page 4, lines 8-15 of the present specification where an inverter generates a power-up signal when VINT rises over a trigger voltage (threshold voltage), VINT causing a gate to close when a threshold voltage is reached, causing the inverter output to change.

Therefore, Parker does not anticipate claim 1 because Parker does not expressly or inherently teach each and every element as set forth in claim 1 (see, e.g., MPEP 2131 - "A

claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.").

Claims 2-5 depend from claim 1. Consequently, Parker also fails to anticipate these claims for at least the reason that Parker does not teach each and every element that is inherent to the claims. MPEP 2131.

Also, Parker does not teach each and every element of claim 10 for at least similar reasons as claim 1. Additionally, Parker fails to teach the element of accessing the semiconductor memory device when the internal voltage has reached an *operational voltage level* (emphasis added). The voltage described in Parker represents *data* inside a NAND memory cell. The voltage thus never reaches an *operational voltage level*. Thus Parker also fails to teach the element of accessing the semiconductor memory device when the internal voltage has reached an *operational voltage level* (emphasis added).

Therefore, Parker does not anticipate claim 10 because Parker does not expressly or inherently teach each and every element as set forth in claim 10 (see, e.g., MPEP 2131 - "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.").

Allowable Subject Matter

Claims 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-9 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Parker (U.S. Patent No. 6,307,783), and others, does not teach the claimed invention having a ready/busy driver controller having level shifter configured to generate the busy enable signal in response to the first and second control signal. Claim 6-9 have been rewritten in independent form and included as new claims 11-14.

New claims

New claims 11-14 have been added. These claims should be allowable because they correspond to claims 6-9 which have been indicated by the Examiner as containing allowable subject matter.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-14 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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Limited Recognition Under 37 CFR § 10.9(b)

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number 703-872-9306, on December 10, 2004.

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